REMARKS

The claims are claims 1 to 6 and 8 to 12.

Claims 1 to 4, 6 and 8 to 12 were rejected under 35 U.S.C. 102(b) as anticipated by Moyer et al U.S. Patent No. 5,375,216.

Claims 1 and 8 recite subject matter not anticipated by Moyer et al. Claim 1 recites "a first requestor," "a second requestor circuit" and "access mode circuitry for indicating at least a first access mode and a second access mode." Claim 8 recites "sharing access to the memory circuit between the plurality of requestor circuits when the digital system is in a first mode of operation" and "limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation." Thus claims 1 and 8 recite both plural requestor circuits and plural modes. The FINAL REJECTION cites portions of Moyer et al of two differing types as anticipating these recitation of claims 1 and 8.

The first type of teaching of Moyer et al cited in the FINAL REJECTION is a single data processor 20 having a single requestor circuit execution unit 42 and two modes, a user mode and a supervisor mode. This teaching of Moyer et al is exemplified in the citations of the FINAL REJECTION to Mcyer et al at: column 1, lines 24 to 38; and column 10, lines 42 to 45 and 49 to 51. Moyer et al states at column 1, lines 21 to 28:

> "In most data processors, two levels of privilege are provided to control access to memory, cache or otherwise, during external bus transactions and to control operation of the data processor. A supervisor mode provides the highest level of privilege. When in supervisor mode, the data processor may access memory designated for both the supervisor mode and a user mode of operation."

Reference to "the data processor" indicates this is singular. Moyer et al states at column 1, lines 43 to 49:

> "For example, in the MC88100 RISC processor available from Motorola, Inc. of Austin, Tex., four instructions are accessible only in the supervisor mode of operation. Three of these instructions execute read/write accesses to a register which may only be accessed when the data processor is in a supervisor mode of operation."

Again reference to "the data processor" implies the singular. Moyer et al states at column 1, lines 52 to 54:

> "If a memory, register, or instruction specified for use only in supervisor mode, is accessed when the data processor is in user mode, an exception may occur."

Moyer et al at column 10, lines 37 to 54 (encompassing two portions cited in the FINAL REJECTION) states:

> "During execution of one of the cache control operations, the SUPERVISOR signal is provided to indicate a mode of operation in which data processor 20 is operating. Assume in the example described herein that the SUPERVISOR signal is negated to indicate that data processor 20 is operating in a user mode. In user mode, access of data cache unit 24 is restricted to only a small portion of memory referred to as 'user memory' and a limited number of registers in register file 32. Additionally, the touch load operation may also be executed in the supervisor mode of operation. If the SUPERVISOR signal is asserted, data processor 20 is operating in the supervisor mode of operation. In the supervisor mode of operation, access to data cache unit 24 and register file 32 is unrestricted. A logic state of the SUPERVISOR signal is determined by sequencer 34 and provided to load/store unit 28 via INTERNAL INFORMATION bus 27."

With plural references to a data processor in the singular and no references to plural data processors, the Applicants respectfully

submit that Moyer et al fails to teach the plural requestor circuits recited in claims 1 and 8.

The second type teaching of Moyer et al cited in the FINAL REJECTION teaches plural requestors but not the recited plural modes. This teaching of Moyer et al is exemplified in the citations of the FINAL REJECTION to Moyer et al at: column 5, lines 9 to 12; and column 11, lines 44 to 46. Moyer et al states at column 5, lines 8to 12:

> "The user may then use the data to control operation of a memory controller, or a similar processing system, to make assumptions about future cache memory transactions."

This disclosure of Moyer et al mentions a possible additional requestor circuit, the memory controller, without any disclosure of the mode limitations recited in claims 1 and 8. This passage thus cannot anticipate these limitations of claims 1 and 8. Moyer et al states at column 11, lines 25 to 52 including the portion cited in the FINAL REJECTION:

> 'The physical address is then used to access a predetermined memory location in data tag array 56. Bits zero through eleven of the effective address are decoded to locate the predetermined memory location in data tag array 56. A data value stored at the predetermined memory location is then compared with bits twelve through thirty-one of the physical address. If identical, data tag array 56 asserts the MATCH signal. Similarly, a status of the data value stored at the memory location is provided via the STATUS signal.
>
> 'The status of the data value may be either invalid, shared unmodified, exclusive modified, or exclusive unmodified. If the status of the data value is invalid, the data value is not the same as a corresponding value in main memory 50. If the status of the data value in data cache 54 is shared unmodified, the data value is shared among other processors (not shown) which are external to data processor 20. However, the data value is the same as a corresponding value in main memory 50. If the status of the data value in data cache 54 is exclusive modified, only data processor 20

> has a copy of the data value. No external processor may access the data value. Additionally, because the data value is modified, the data value is 'dirty,' or different than a corresponding value in main memory 50. Lastly, if the status of the data value is exclusive unmodified, only data processor 20 has a copy of the data value, and the data value is the same as a corresponding value in main memory 50."

This portion of Moyer et al teaches plural requestor circuits, the data processor and at least one "external processor." This portion of Moyer et al also teaches limitations upon access to the memory. However, the limitation upon access is based upon different criteria than recited in claims 1 and 8. Claims 1 and 8 recite limitations on access dependent upon access mode. This portion of Moyer et al instead teaches limitations upon access based upon status data stored in data tag array 56. Moyer et al teaches that this status data is stored in a memory location within data tag array 56 corresponding to the physical address of the data access. Because of this manner of storing the status, differing locations within the cache can have differing status. Thus the external processor may have access to some data and not to other data stored in the cache dependent upon the corresponding status in data tag array 56. This is contrary to the recitations of claims 1 and 8, which determine access dependent upon a mode. Accordingly, claims 1 and 8 are allowable over Moyer et al.

Claims 1 and 8 recite further subject matter not anticipated by Moyer et al. Claim 1 recites "the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode." Claim 8 recites "selecting a first portion of the memory circuit...such that a second portion of the memory circuit

is not selected." The FINAL REJECTION cites column 4, lines 61 to 63, column 10, lines 55 to 59 and column 18, lines 62 to 67 of Moyer et al as anticipating this subject matter. Moyer et al states at column 4, lines 61 to 63:

> "Each of the cache control instructions described above is encoded as a load operation having a predetermined size access to a predetermined register."

Moyer et al states at column 10, lines 55 to 59:

> "The SIZE signal indicates whether a memory access should be in byte, halfword, word, or double word increments. The SIZE signal is typically encoded in the instruction opcode provided by instruction cache unit 16."

Moyer et al at column 18, lines 62 to 67 merely mentions a SIZE signal without further elaboration. The Applicants respectfully submit that these portions of Moyer et al disclose that the data size is the size of data movement "word increments" and not the size of a portion of memory as recited in claims 1 and 8. Note especially that a memory size of a byte, a halfword, a word or a double word would be impractical to support the data accesses recited in claims 1 and 8. However, such data accesses could easily be made in "word increments" of a byte, a halfword, a word or a double word as recited in Moyer et al. Accordingly, claims 1 and 8 are not anticipated by Moyer et al.

Claims 1 and 8 recite further subject matter not anticipated by Moyer et al. Claim 1 recites "a size register for holding a size parameter coupled to the selection circuit." Claim 8 recites "a size parameter stored in a register." Thus these claims require the size parameter to be stored in a register. In contrast, the portion of Moyer et al cited in the FINAL REJECTION (quoted above) recites "The SIZE signal is typically encoded in the instruction

opcode provided by instruction cache unit 16." The Applicants respectfully submit that encoding the SIZE signal in an instruction opcode does not anticipate storing this parameter in a register. Accordingly, claims 1 and 8 are not anticipated by Moyer et al.

Claims 2 and 10 recite subject matter not anticipated by Moyer et al. Claim 2 recites "wherein a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode." Claim 10 recites "placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation." The FINAL REJECTION states at page 5, lines 6 to 8:

> "said second portion would inherently placed in low power mode as it is not being addressed and the location pertaining to the second portion is not activated"

This part of Moyer et al fails to teach that any portion of memory is powered differently based upon the mode. If the Examiner's reasoning is to be believed, then the user memory would also be in a low power state if it is not currently being accessed. The Applicants respectfully submit that the recitations of claims 2 and 10 quoted above mean more than that the memory portion is not currently being accessed. Accordingly, claims 2 and 10 are not anticipated by Moyer et al.

Claim 4 recites subject matter not anticipated by Moyer et al. Claim 4 recites "wherein the size parameter is ignored when the access mode circuitry indicates the first access mode such that the entire memory circuit is operable to be selected for sequential access by the first requestor and the second requestor." Moyer et al includes no teaching that the size may be ignored in one mode and not ignored in another mode. The portions of Moyer et al cited as teaching the size limitation include no teaching of this

limitation of claim 4. The FINAL REJECTION fails to cite any portion of Moyer et al as anticipating this subject matter. Accordingly, claim 4 is allowable over Moyer et al.

Claim 6 recites subject matter not anticipated by Moyer et al. Claim 6 recites "the second requester circuit is direct memory access circuit channel controller." The Applicants respectfully submit that Moyer et al fails to teach a direct memory access channel controller. In addition, the FINAL REJECTION fails to allege that Moyer et al teaches such an element. Accordingly, claim 6 is not anticipated by Moyer et al.

Claim 12 recites subject matter not anticipated by Moyer et al. Claim 12 recites "storing a different size parameter in the register, such that the step of selecting results in a first portion having a different size in response to the different size parameter." As noted above, Moyer et al teaches that the SIZE parameter is "encoded in the instruction opcode." The Applicants respectfully submit that this teaching of Moyer et al negates any inference that the size parameter can be changed by writing to a register as recited in claim 12. Further, the FINAL REJECTION fails to allege that Moyer et al teaches this subject matter. Accordingly, claim 12 is not anticipated by Moyer et al.

Paragraph 5 of page 5 of the FINAL REJETION stated that claim 5 is allowable.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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